Electronic Version
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Claims

[c1] 1.A chip package structure, comprising:
a substrate, having a lateral surface, a first surface and a second surface, wherein the substrate further has a first metallic layer, a second metallic layer and a conductor with the first metallic layer located on the first surface of the substrate, the second metallic layer located on the second surface of the substrate and the conductor located on the lateral surface of the substrate, and the first metallic layer is electrically connected to the second metallic layer through the conductor;
a lead frame, located on the first surface of the substrate, wherein the lead frame is electrically connected to the first metallic layer;
a first chip, having a first active surface and a first back surface, wherein the first back surface of the first chip is bonded either onto the surface of the lead frame or onto the first surface, and the first chip has a plurality of first bonding pads on the first active surface;
a plurality of first bonding wires, connecting the first bonding pads of the first chip to the lead frame;
a heat sink, located on the second surface and electrically connected to the second metallic layer; and

a packaging material, encapsulating the first chip, the first bonding wires and a portion of the lead frame, the lead frame having another portion exposed to the ambient.

[c2] 2. The chip package structure of claim 1, wherein the conductor comprises a copper layer.

[c3] 3. The chip package structure of claim 1, wherein the conductor has a thickness ranging from 0.1μm to 5μm.

[c4] 4. The chip package structure of claim 1, wherein the conductor is fabricated using a conductive adhesive.

[c5] 5. The chip package structure of claim 1, wherein the process of fabricating the conductor comprises sputtering, evaporation plating, chemical vapor deposition, electroplating or coat-spreading.

[c6] 6. The chip package structure of claim 1, further comprising a second chip and a plurality of second bonding wires, wherein the second chip is bonded either onto the lead frame or onto the first surface of the substrate, and the second bonding wires connects the second chip to the lead frame, and the packaging material further encapsulates the second chip and the second bonding wires.

[c7] 7. The chip package structure of claim 6, further comprising a plurality of third bonding wires connecting the first chip to the second chip.

[c8] 8. The chip package structure of claim 1, wherein the substrate has an insulating layer fabricated using a ceramic material.

[c9] 9. A substrate structure with a lateral surface, a first surface and a second surface, comprising:
a first metallic layer, located on the first surface of the substrate;
a second metallic layer, located on the second surface of the substrate; and
a conductor, located on the lateral surface of the substrate, wherein the first metallic layer is electrically connected to the second metallic layer through the conductor.

[c10] 10. The substrate structure of claim 9, wherein the conductor comprises a copper layer.

[c11] 11. The substrate structure of claim 9, wherein the conductor has a thickness ranging from 0.1μm to 5μm.

[c12] 12. The substrate structure of claim 9, wherein the conductor is fabricated using a conductive adhesive.

[c13] 13. The substrate structure of claim 9, wherein the process of fabricating the conductor comprises sputtering, evaporation plating, chemical vapor deposition, electroplating or coat-spreading.

[c14] 14. The substrate structure of claim 9, wherein the substrate has an insulating layer fabricated using a ceramic material.